

Claims

[c0001] 1. A multi-layered lithography structure, the structure comprising: a substrate; a first resist layer with a first surface coupled to said substrate, said first resist layer having a first resist open area; a barrier layer on a second surface of said first resist with a barrier layer open area; a second resist layer coupled to said barrier layer, said second resist layer having a second resist open area; and wherein said first resist open area is subject to develop subsequent to develop of said second resist open area.

[c0002] 2. The structure of claim 1, further comprising a second barrier layer on said second resist layer with a second barrier layer open area, and a third resist layer on said second barrier layer with a third resist open area, wherein said second resist open area is subject to develop subsequent to develop of said third resist open area.

[c0003] 3. The structure of claim 1, wherein said first resist open area, said barrier layer open area, and said second resist open area have variable patterns.

[c0004] 4. The structure of claim 1, further comprising a plurality of said structures on said substrate.

[c0005] 5. The structure of claim 1, wherein said first resist open area, said barrier layer open area, said second resist open area have variable sizes.

[c0006] 6. The structure of claim 1, wherein said barrier layer is an opaque metallic layer.

[c0007] 7. The structure of claim 1, wherein said first resist layer and said second resist layer are selected from at least one of the group consisting of: azide, polymers and copolymers of polymethylmethacrylate (PMMA), and SU-8.

[c0008] 8. The structure of claim 1 wherein said substrate is selected from at least one of the group consisting of: silicon, gallium arsenide, germanium, glass, and metal.

[c0009] 9. A method of fabricating a multi-layer lithographic semiconductor, comprising: applying a first resist layer to a semiconductor substrate; masking said first resist layer and exposing said first resist layer, thereby forming a first latent image in said first resist layer; adding a barrier layer to said first resist layer covering said first latent image; applying a second resist layer to said barrier layer; masking said second resist layer and exposing

said second resist layer, thereby forming a second latent image in said second resist layer; removing said second latent image; etching said barrier layer; and removing said first latent image.

[c0010] 10. The method of claim 9, further comprising preparing said substrate.

[c0011] 11. The method of claim 9, further comprising applying post-application resist treatments.

[c0012] 12. The method of claim 11, wherein said post-application resist treatments are selected from at least one of the group consisting of: softbake, hydration, and ammonia based image reversal.

[c0013] 13. The method of claim 9, wherein a shape of said first latent image and the second latent image is selected from the group consisting of: square, rectangle, triangle, circle, oval, and polygon.

[c0014] 14. The method of claim 9, wherein said etching is selected from the group consisting of wet etch, dry etch and develop/exposure.

[c0015] 15. The method of claim 9, wherein said exposing uses rays selected from at least one of the group consisting of ultraviolet light, electrons, and x-rays.

[c0016] 16. The method of claim 9, further comprising using alignment tools.

[c0017] 17. The method of claim 9, further comprising adding a second barrier layer on said second resist layer, applying a third resist layer on said second barrier layer, masking said third resist layer and exposing said third resist layer, thereby forming a third latent image in said third resist layer, removing said third latent image, etching said second barrier layer, and removing said second latent image.

[c0018] 18. A lithographic process for fabricating multi-layer semiconductor devices, comprising: providing a substrate; coating a first resist layer onto said substrate; exposing said first resist layer with a mask to form a first layer exposed area and a first layer unexposed area; depositing a barrier layer on said first layer exposed area and said first layer unexposed area; coating a second resist layer onto said barrier layer; exposing said second resist layer with a mask to form a second layer exposed area and a second layer unexposed area; developing said second layer exposed area; etching said barrier layer; developing said first layer exposed area; and fabricating devices on said substrate.

[c0019] 19. The lithographic process according to claim 18,
wherein said depositing is selected from the group con-
sisting of: thermal evaporation, spin coating, spray coat-
ing, and electroless plating.

[c0020] 20. The lithographic process according to claim 18,
wherein said step of coating is spun coating.